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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/724,387	INUKAI, KAZUTAKA	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37

CFR 3.73(b).

1. Claims 1-67 are rejected under the judicially created doctrine of non-obviousness-type double patenting as being unpatentable over claims 1-49 of U.S. Patent No. 6,548,960. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are pertain to the same invention with some parts being duplicated, like switching TFTs, driver TFTs and eliminating TFTs.

Claim 1 of this application 09/724/387	**Claim 1 of the US 6,548,960 B2**
An electronic device comprising:	An electronic device comprising:
a source signal line driver circuit;	a pair of source signal line driver circuits;
a first gate signal line driver circuit;	a pair of gate signal line driver circuits; and
a second gate signal driver circuit; and	
a pixel portion including a plurality of pixels,	a pixel portion including a plurality of pixels,
wherein plurality of pixels each have	wherein plurality of pixels each have

an EL element, an EL driving TFT controlling luminescence of each of the EL elements, a switching TFT, and an eliminating TFT for controlling EL driving TFT, wherein switching TFT is controlled by first gate signal driver circuit, and wherein a gray-scale display is performed by controlling a luminescing time of plurality of EL elements.	an EL element, pair of EL driving TFTs, pair of switching TFTs and pair of eliminating TFTs, wherein luminescence of the EL element is controlled by pair of driver TFTs; wherein one of the pair of EL driver TFTs is controlled by one of pair of switching TFTs and one of pair of eliminating TFTs, wherein the other of pair of EL driver TFTs is controlled by the other of pair of switching TFTs and the other of eliminating TFTs, and wherein a gray-scale display is performed by controlling a luminescing time of plurality of EL elements.

Note the comparison above, claims 1, 7, 13, 60, 64 of the instant invention is not patentably distinct from claim 1, of US Patent No. 6,548,960 B2. for example, claim 1 of the instant application differs only in that some parts being duplicated in US Patent No. 6,548,960 B2.

As to dependent claims 3-6, 8-12, 61-63, 65-67, these claims are duplicate claims 2-14 of US Patent No. 6,548,960 B2.

Claim 22 of this application 09/724/387	**Claims 15, 18 of the US 6,548,960 B2**
An electronic device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, a pixel portion including a plurality of pixels, a plurality of source signal lines connected to said source signal line driver circuit, a plurality of first gate signal lines connected to said first gate signal line driver circuit, a plurality of second gate signal lines connected to said second gate signal line driver circuit, and a power supply line, wherein said plurality of pixels each have a switching TFT, an EL driving TFT, an eliminating TFT, and an EL element; a gate electrode of said switching TFT is connected to said first gate signal lines; one of a source region and a drain region of said switching TFT is connected to said plurality of source signal lines, and another thereof is connected to a gate electrode of said EL driving TFT; a gate electrode of said eliminating	An electronic device comprising a first and second gate and source driver circuits, a pixel portion including a plurality of pixels, a plurality of first and second source signal lines connected to first, 2nd gate signal line driver circuit, and a power supply line, wherein said plurality of pixels each have first and 2nd switching TFT, 1st and 2nd eliminating TFT, 1st and 2nd driver, an EL element; wherein a gate electrodes 1st and 2nd switching TFT is connected 1st and 2nd gate signal line, one of a source region and a drain of 1st and 2nd TFT is connected to 1st and 2nd source lines and another is connected to gate,

TFT is connected to said second gate signal lines; TFTs are one of a source region and a drain region of said eliminating TFT is connected to said power supply line, and another thereof is connected a gate electrode of said EL driving TFT; one of a source region and a drain region EL driving TFT is connected to said power supply line, and another thereof is connected to connected to EL; element; an (n) number of writing-in periods Tal, Ta2, ..., Ta(n) and an (m-1) number (m-1) eliminating periods Tel, Te2, ..., Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period; digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in periods the digital data signals fed to said entire plurality of pixels are all eliminated in said eliminating periods Tel, Te2, ..., Te(m-1);

gate electrodes of eliminating TFTs are connected to1st and 2nd gate signal lines; a source region and a drain region of eliminating TFTs is connected to power supply, one of a source region and a drain region EL driving TFT is connected to power supply line, and another an (n) number of writing-in periods Tal, Ta2, ..., Ta(n) and an (m-1) eliminating periods Tel, Te2, ..., Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period; digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in the digital data signals fed to said entire plurality of pixels are all eliminated in eliminating periods Tel, Te2, ..., Te(m-1);

among said (n) number of writing-in periods among said (n) number of writing-in periods

Tal, Ta2, ..., Ta(n), a portion of the writing-in periods Tal, Ta2, ..., Ta(n), a portion of the writing-in periods Tal, Ta2, ..., Ta(m) and a portion of said eliminating periods Tel, Te2, ..., Te(m-1) periods from the start of each of the writing-in periods Tal, TA, ..., Ta(m-1) in said (n) number of writing-in periods Tal, Ta2, ..., Ta(n) to the start of each of said eliminating periods Tel, Te2, ..., Te(m-1) are display periods Trl, Tr2, ..., Tr(m-1);

periods from the start of each of said eliminating periods Tel, Te2, ..., Te(m-1) to the start of each of the writing-in periods Tal, Ta2, ..., Tatm) in said (n) nllmber of writing-in periods Tal, Ta2, ..., Tatn) are non-display periods Tdl, Td2, ..., Td(m-1);

periods from the start of each of the writing-in periods Tal, Ta2, ..., Ta(m+1) in said (n) number of writing-in periods Tal, TA, ..., Tatn) to the start of the next writing-in periods of each of said writing-in periods Ta(m), Ta(m+1), ...,

Tal, Ta2, ..., Ta(n), a portion of the Ta(m) and a portion of eliminating periods Tel, Te2, ..., Te(m-1) periods from the start of each of the Tal, TA, ..., Ta(m-1) in said (n) number of writing-in periods Tal, Ta2, ..., Ta(n) to the start of each of eliminating periods Tel, Te2, ..., Te(m-1) are display periods Trl, Tr2, ..., Tr(m-1);

periods from the start of each of said eliminating periods Tel, Te2, ..., Te(m-1) the start of each of the writing-in periods Ta2, ..., Tatm) in said (n) nllmber of writing-in periods Tal, Ta2, ..., Tatn) are non-display periods Tdl, Td2, ..., Td(m-1);

periods from the start of each of the Tal, Ta2, ..., Ta(m+1) in said (n) number of writing-in periods Tal, TA, ..., to the start of the next writing-in of of said writing-in periods Ta(m), Ta(m+1),

Ta(n), respectively, are display periods Tr(m), periods Tr(m+1), ..., Tr(n);	Ta(n), respectively, are display Tr(m), Tr(m+1), ..., Tr(n);
in said display periods Trl, Tr2, ..., Tr(n), said plurality of EL elements are selected by said digital data signals to luminesce or not luminesce;	in said display periods Trl, Tr2, ..., Tr(n), plurality of EL elements are selected by digital data signals to luminesce or a not
length of said (n) number of writing-in periods in Tal, Ta2, ..., Tatn) and a length of said (m-1) number of eliminating periods Tel, Te2, ..., Te(m-1) are the same; and	a length of said (n) number of writing- Ta2, ..., Tatn) and a length of said m-1) number of eliminating periods Tel, Te2, ..., Te(m-1) are the same; and
0 . .g 1	0 . .g 1 . . . . .
ratios of the length of said display periods Trl, Tr2, ..., Trtn) are expressed as 2 . . .	ratios of the length of said display periods Trl, Tr2, ..., Trtn) are expressed as 2 . . .

Note the comparison above, claims 22, 30, 41, 40 and 49 of the instant invention is not patentably distinct from claims 15, 18, of US Patent No. 6,548,960 B2, for example, claim 22 of the instant application differs only in that some parts being duplicated in US Patent No. 6,548,960 B2.

As to dependent claims 23-29, 31-40, 42-48, 50-59 these claims are duplicate claims 16-17, 19-49 of US Patent No. 6,548,960 B2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, 7-8, 10, 13-15, 17, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US Patent No. 5,990,629) in view of Sano (US Patent No. 6,246,384).

As to claim 1, Yamada et al. teaches an electronic device (See Fig. 1, Col. 1, Lines 5-9) comprising:

a source line driver circuit (See Fig. 1, item 4, Col. 5, Lines 46-51 and Fig. 17, item 4, Col. 29, Lines 35-58);

a first gate signal line driver circuit (in the reference equivalent to gate driver) (See Fig. 1, item 2, Col. 5, Lines 46-51 and Fig. 17, item 2, Col. 29, Lines 35-58);

a second gate signal line driver circuit (equivalent in the reference to common driver) (See Fig. 1, item 5, Col. 5, Lines 46-51 and Fig. 17, item 5, Col. 29, Lines 35-58); and

a pixel portion including plurality of pixels (Fig. 17, items 51-53, Cp, Col. 29, Lines 40-43);

wherein plurality of pixels each have an EL element (Fig. 17, item 51, Col. 29, Lines 40-43), an EL driving TFT for controlling luminescence of each of the El

elements (Fig. 17, item 52, Col. 29, Lines 40-43), a switching TFT (in the reference "a selection transistor") (Fig. 17, item 53, Col. 29, Lines 40-43),

wherein switching TFT is controlled by first gate signal line driver circuit (See Fig. 17, items 3, 53, GL, Col. 29, Lines 44-49), and

wherein a gay-scale display is performed by controlling a luminescent time of plurality of EL elements (See Fig. 5, item 2m, Col. 13, Lines 13-57 and Table 1).

Yamada et al. does not disclose an eliminating TFT for controlling EL driving TFT controlled by second gate driver.

Sano teaches an eliminating TFT for controlling EL driving TFT (See Fig. 2, item 56, Col. 5, Lines 45-50), controlled by second driver (See Fig. 3, item Vg4, Col. 5, Lines 45-50).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Sano into the Yamada et al. system in order to enable the current supply to the EL device to be controlled (See Col. 2, Lines 35-40 in the Sano reference).

As to claims 2, 8, 17 Yamada et al. teaches switching and EL driving TFTs are at least one of a N channel or a P channel TFTs (See Fig. 1, item 12-13, Col. 6, Lines 57-62) and Shiotani et al. teaches eliminating TFTs are at least one of a N channel or a P channel TFTs (See Drawing 8, items S2, Q4, in Detailed description See page 6, paragraphs 0026-0027).

As to claims 4, 10, 19 Yamada et al. teaches a computer, which uses electronic device (See Col. 13, Lines 53-57).

As to claim 7, Yamada et al. teaches an electronic device (See Fig. 1, Col. 1, Lines 5-9) comprising:

a source line driver circuit connected to a plurality of source signal lines (See Fig. 1, item 4, Col. 5, Lines 46-51 and Fig. 17, items 4, Y1, Y2,..., Col. 29, Lines 35-58);

a first gate signal line driver (in the reference equivalent to gate driver) circuit connected to a plurality of first gate signal lines (in the reference equivalent to gate signal lines) (See Fig. 1, item 2, Col. 5, Lines 46-51 and Fig. 17, items 2, X1, X2,..., Col. 29, Lines 35-58);

a second gate signal line driver circuit (equivalent in the reference to common driver) connected to a plurality of second gate signal lines (equivalent in the reference to common signal lines) (See Fig. 1, item 5, Col. 5, Lines 46-51 and Fig. 17, items 5, Z1, Z2,...,Col. 29, Lines 35-58); and

a pixel portion including plurality of pixels (Fig. 17, items 51-53, Cp, Col. 29, Lines 40-43);

wherein plurality of pixels each have an EL element (Fig. 17, item 51, Col. 29, Lines 40-43), an EL driving TFT for controlling luminescence of each of the El elements (Fig. 17, item 52, Col. 29, Lines 40-43), a switching TFT (in the reference "a selection transistor") (Fig. 17, item 53, Col. 29, Lines 40-43),

wherein switching TFT is controlled by first gate signal line driver circuit (See Fig. 17, items 3, 53, GL, Col. 29, Lines 44-49), and

wherein a gay-scale display is performed by controlling a luminescent time of plurality of EL elements (See Fig. 5, item 2m, Col. 13, Lines 13-57 and Table 1).

Sano teaches an eliminating TFT for controlling EL driving TFT (See Fig. 2, item 56, Col. 5, Lines 45-50), controlled by second driver (See Fig. 3, item Vg4, Col. 5, Lines 45-50).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Sano into the Yamada et al. system in order to enable the current supply to the EL device to be controlled (See Col. 2, Lines 35-40 in the Sano reference).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Shiotani et al. into the Yamada et al. system and control eliminating TFT by second gate driver circuit in order to enable gradational representation (See Abstract in the of Shiotani et al. reference).

As to claim 13, Yamada et al. teaches an electronic device (See Fig. 1, Col. 1, Lines 5-9) comprising:

a source line driver circuit connected to a plurality of source signal lines (See Fig. 1, item 4, Col. 5, Lines 46-51 and Fig. 17, items 4, Y1, Y2,..., Col. 29, Lines 35-58);

a first gate signal line driver (in the reference equivalent to gate driver) circuit connected to a plurality of first gate signal lines (in the reference equivalent to gate signal lines) (See Fig. 1, item 2, Col. 5, Lines 46-51 and Fig. 17, items 2, X1, X2,..., Col. 29, Lines 35-58);

a second gate signal line driver circuit (equivalent in the reference to common driver) connected to a plurality of second gate signal lines (equivalent in the reference to common signal lines) (See Fig. 1, item 5, Col. 5, Lines 46-51 and Fig. 17, items 5, Z1, Z2,...,Col. 29, Lines 35-58); and

a pixel portion including plurality of pixels (Fig. 17, items 51-53, Cp, Col. 29, Lines 40-43);

wherein plurality of pixels each have an EL element (Fig. 17, item 51, Col. 29, Lines 40-43), an EL driving TFT for controlling luminescence of each of the El elements (Fig. 17, item 52, Col. 29, Lines 40-43), a switching TFT (in the reference "a selection transistor") (Fig. 17, item 53, Col. 29, Lines 40-43),

wherein EL element includes a pixel electrode, an opposing electrode held at a constant electric potential, and an EL layer formed between pixel electrode and opposing electrode (See Fig. 17, item 51, from Col. 29, Line 66 to Col. 30, Line 6);

wherein a gate electrode of switching TFT is connected to first gate signal lines (See Fig. 17, items 53, GL, Col. 29, Lines 44-49), and

wherein one of a source region and a drain region of switching TFT is connected to plurality of source signal lines, and another is connected to a gate electrode of El driving TFT (See Fig. 17, items 52-53, Col. 29, Lines 40-44),

wherein one of a source region and a drain region of EL driving TFT is connected to the power supply line (in the reference common driver lines) (See Fig. 17, items 52, Z1, Z2, ...,) and another is connected to a pixel electrode of EL element (See Fig. 17, items 51-52, Col. 29, Lines 35-59).

Sano teaches an eliminating TFT for controlling EL driving TFT (See Fig. 2, item 56, Col. 5, Lines 45-50), controlled by second driver (See Fig. 3, item Vg4, Col. 5, Lines 45-50).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Sano into the Yamada et al. system in order to enable the current supply to the EL device to be controlled (See Col. 2, Lines 35-40 in the Sano reference).

As to claims 14-15, Yamada et al. teaches EL layer is low molecular organic material is made of Alq3 (See Col. 8, Lines 26-31).

3. Claims 5, 11, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. and Sato as applied to claims 1, 7, 13 above, and further in view of Chiu (US Patent No. 5,606,348).

Yamada et al. and Sato do not show video camera which uses electronic device according to claim 1.

Chiu teaches EL device used to display video camera signals (See Col. 2, Lines 33-46).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Chui into Sato and the Yamada et al. system in order to enable gradational representation.

4. Claims 6, 12, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. and Sato as applied to claims 1, 7, 13 above, and further in view of Okayama et al. (US Patent No. 5,899,575).

Yamada et al. and Shiotani et al. do not show DVD player which uses electronic device according to claim 1.

Okayama et al. teaches EL device used to display DVD player signals (See Col. 6, Lines 19-36).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Okayama et al. into Sato and the Yamada et al. system in order to enable gradational representation.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. and Sato as applied to claim 13 above, and further in view of Hsieh (US Patent No. 5,876,865).

Yamada et al. and Shiotani et al. do not show polymer organic material is made of PPV.

Hsieh teaches polymer organic material is made of PPV (See Col. 2, Lines 7-33).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Hsieh into Sato and the Yamada et al. system in order to enable gradational representation.

6. Claim 60-61, 64-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osada et al. (US Patent No. 6,504,520 B1) in view of Yamada et al. and Sato.

As to claim 60, Osada et al. teaches an electronic device (See Col. 1, Lines 16-20) comprising a source signal line driver circuit (See Fig. 1, item 4, Col. 3, Lines 34-55), a first gate signal driver circuit (See Fig. 1, item 2, Col. 3, Lines 34-55), a second gate signal line driver circuit (See Fig. 1, item 3, Col. 3, Lines 34-55), and a pixel portion including a plurality of pixels (See Fig. 1, item 1, Col. 3, Lines 34-66),

wherein plurality of pixels have a plurality of EL elements (See Fig. 1, item 3, Col. 3, Lines 34-40), and wherein respective drives of plurality of EL elements are controlled by a signal outputted from source signal line driver circuit (See Fig. 1, item 4, Col. 3, Lines 56-66), a first selecting signal outputted from first gate signal line driver circuit (See Fig. 1, item 2, Col. 3, Lines 56-66), and a second selecting signal outputted from second gate signal line driver circuit (See Fig. 1, item 3, Col. 3, Lines 56-66).

Osada et al. does not show EL elements are controlled by a digital data signal.

Yamada et al. teaches EL elements are controlled by a digital data signal (See Fig. 5, item 2l, Table 1, Col. 10, Lines 41-51),

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Yamada et al. into Osada et al. system in order to provide an EL display apparatus with high image quality (See Col. 2, Lines 10-16 in the Yamada et al. reference).

Osada et al. and Yamada et al. do not disclose the second TFT connected to the second gate signal driver circuit.

Sano teaches an eliminating TFT for controlling EL driving TFT (See Fig. 2, item 56, Col. 5, Lines 45-50), controlled by second driver (See Fig. 3, item Vg4, Col. 5, Lines 45-50).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Sano into the Osada et al., Yamada et al. system in order to enable the current supply to the EL device to be controlled (See Col. 2, Lines 35-40 in the Sano reference).

As to claim 64, Osada et al. teaches an electronic device (See Col. 1, Lines 16-20) comprising a source signal line driver circuit (See Fig. 1, item 4, Col. 3, Lines 34-55), a first gate signal driver circuit (See Fig. 1, item 2, Col. 3, Lines 34-55), a second gate signal line driver circuit (See Fig. 1, item 3, Col. 3, Lines 34-55), and a pixel portion including a plurality of pixels (See Fig. 1, item 1, Col. 3, Lines 34-66),

wherein plurality of pixels have a plurality of EL elements (See Fig. 1, item 3, Col. 3, Lines 34-40), and wherein respective drives of plurality of EL elements are controlled by a signal outputted from source signal line driver circuit (See Fig. 1, item 4, Col. 3, Lines 56-66), a first selecting signal outputted from first gate signal line driver circuit (See Fig. 1, item 2, Col. 3, Lines 56-66), and a second selecting signal outputted from second gate signal line driver circuit (See Fig. 1, item 3, Col. 3, Lines 56-66).

Osada et al. does not show EL elements, wherein a luminescent time is controlled by a digital data signal to perform gray-scale display.

Yamada et al. teaches EL elements, wherein a luminescent time is controlled by a digital data signal to perform gray-scale display (See Fig. 5, item 2l, Table 1, Col. 10, Lines 41-51),

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Yamada et al. into Osada et al. system in order to provide an EL display apparatus with high image quality (See Col. 2, Lines 10-16 in the Yamada et al. reference).

Osada et al. and Yamada et al. do not disclose the second TFT connected to the second gate signal driver circuit.

Sano teaches an eliminating TFT for controlling EL driving TFT (See Fig. 2, item 56, Col. 5, Lines 45-50), controlled by second driver (See Fig. 3, item Vg4, Col. 5, Lines 45-50).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Sano into the Osada et al., Yamada et al. system in order to enable the current supply to the EL device to be controlled (See Col. 2, Lines 35-40 in the Sano reference).

As to claims 61, 65 Yamada et al. teaches a computer, which uses electronic device according to claims 60, 64 (See Col. 13, Lines 53-57).

7. Claims 62, 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. and Osada et al., Sano as applied to claims 60, 64 above, and further in view of Chiu (US Patent No. 5,606,348).

Yamada et al. and Osada et al. do not show video camera which uses electronic device according to claim 1.

Chiu teaches EL device used to display video camera signals (See Col. 2, Lines 33-46).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Chui into Osada et al. and the Yamada et al., Sato system in order to enable gradational representation.

8. Claims 63, 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. and Osada et al., Sano as applied to claims 60, 64 above, and further in view of Okayama et al. (US Patent No. 5,899,575).

Yamada et al. and Osada et al., Sano do not show DVD player which uses electronic device according to claim 1.

Okayama et al. teaches EL device used to display DVD player signals (See Col. 6, Lines 19-36).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Okayama et al. into Osada et al., Sano and the Yamada et al. system in order to enable gradational representation.

Response to Arguments

9. Applicant's arguments filed on 12. 10.04 with respect to claims 1-2, 4-8, 10-17, 19-21, 60-67 have been considered but are moot in view of the new ground(s) of rejection.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
06.21.05

VIJAY SHANKAR
PRIMARY EXAMINER